MEMORY MODELING CIRCUIT WITH FAULT TOLERATION

ABSTRACT OF THE INVENTION

A memory modeling circuit with fault toleration includes a compare circuit, a control circuit and a test circuit. The compare circuit receives the data stored in the same address of memories and compares data with each other to produce the correct reading data. The control circuit connects with the control signals of the memories and detects that control signals. The control circuit has data output/input ports. When the control signal of the memories is to write, the control circuit enters a writing mode and writes the writing data received from the data output/input ports in the same address of the memories. When the control signal of the memories is to read, the control circuit enters a reading mode, receiving the reading data generated by the compare circuit and outputs it through the data output/input ports. The test circuit receives the data stored in the same address of the memories and the reading data generated by the compare circuit to generate a testing result. The testing result can identify a faulty memory or a faulty compare circuit.